IN THE CLAIMS

1. (previously presented): A non-optical electronic semiconductor device comprising:

a sapphire support substrate including at least one groove;

a first insulation layer on top of the support substrate;

an SOI layer formed on top of the first insulation layer;

a first element layer formed on the SOI layer,

wherein the at least one groove extends below a target element in the first element layer whose dielectric loss is to be controlled;

a second insulation layer formed on top of the first element layer; and

at least one additional element layer formed on top of the second insulation layer.

2. (previously presented): The semiconductor device according to claim 1, wherein the at least one groove is formed such that a lower face of the first insulation layer is exposed.

3. (previously presented): The semiconductor device according to claim 1, wherein the target element is an analog element.

4. (original): The semiconductor device according to claim 3, wherein the analog element is an inductor.

5. (canceled)

6. (previously presented): A non-optical electronic semiconductor device comprising:

a sapphire support substrate including at least one groove;

a first insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer;

a plurality of analog elements formed on the SOI layer,

wherein the at least one groove extends below one or more analog elements among the plurality of analog elements;

a second insulation layer formed over the plurality of analog elements; and

at least one additional element layer formed on top of the second insulation layer.

7. (previously presented): The semiconductor device according to claim 6, wherein the groove is formed such that a lower face of the first insulation layer is exposed.

8. (previously presented): The semiconductor device according to claim 6, wherein the one or more analog elements are inductors.

9. (previously presented): The semiconductor device according to claim 6, wherein the one or more analog elements are elements for which control of dielectric loss is sought, among the plurality of analog elements.

10.-20. (canceled)

21. (previously presented): A non-optical electronic semiconductor device comprising:

a support substrate including at least one groove;

a first insulation layer on top of the support substrate;

an SOI layer formed on top of the first insulation layer;

a first element layer formed in a first-element area on the SOI layer,

wherein the at least one groove extends below a target element in the first element layer whose dielectric loss is to be controlled;

a second insulation layer formed on top of the first element layer; and

at least one additional element layer formed on top of the second insulation layer;

the substrate further comprising a plurality of bonding pads surrounding the first-element area; and

wherein no groove is formed below the plurality of bonding pads.

22. (previously presented): The semiconductor device according to claim 21, wherein the target element is a high-frequency circuit.

23. (previously presented): The semiconductor device according to claim 21, wherein the support substrate is a sapphire substrate.

24. (previously presented): The semiconductor device according to claim 21, wherein the at least one groove is formed such that a lower face of the first insulation layer is exposed.

25. (previously presented): The semiconductor device according to claim 21, wherein the target element is an analog element.

26. (previously presented): The semiconductor device according to claim 25, wherein the analog element is an inductor.

27. (previously presented): A non-optical electronic semiconductor device comprising:

a support substrate including at least one groove;

a first insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer;

a plurality of analog elements formed in an analog-element area on the SOI layer,

wherein the at least one groove extends below one or more analog elements among the plurality of analog elements;

a second insulation layer formed over the plurality of analog elements; and

at least one additional element layer formed on top of the second insulation layer;

the substrate further comprising a plurality of bonding pads surrounding the analog-element area; and

wherein no groove is formed below the plurality of bonding pads.

28. (previously presented): The semiconductor device according to claim 27, wherein said one or more analog elements are inductors.

29. (previously presented): The semiconductor device according to claim 27, wherein said one or more analog elements are elements for which control of dielectric loss is sought.

30. (previously presented): The semiconductor device according to claim 27, wherein the support substrate is a sapphire substrate.

31. (new): The semiconductor device according to claim 21, wherein the at least one groove extends below the entire first-element area, whereby the groove extends below target elements and other elements in the first-element area, except for the bonding pads, whereby rigidity of the support substrate is maintained.

32. (new): The semiconductor device according to claim 27, wherein the at least one groove extends below the entire analog-element area, whereby the groove extends below analog elements and other elements, except for the bonding pads, whereby rigidity of the support substrate is maintained.